

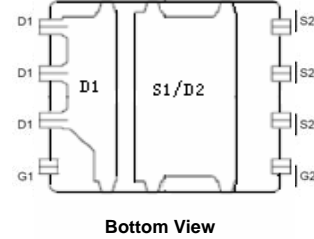
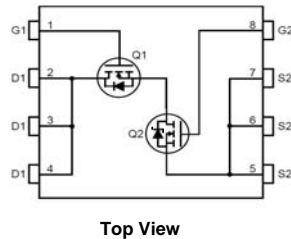
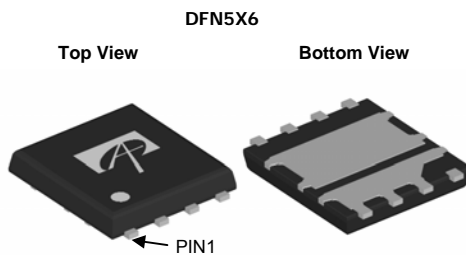
General Description

The AON6926 is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two specialized MOSFETs in a dual Power DFN5x6A package. The Q1 "High Side" MOSFET is designed to minimize switching losses. The Q2 "Low Side" MOSFET is an SRFET™ that features low $R_{DS(ON)}$ to reduce conduction losses as well as an integrated Schottky diode with low Q_{RR} and V_f to reduce switching losses. The AON6926 is well suited for use in compact DC/DC converter applications.

Product Summary

	Q1	Q2
V_{DS}	30V	30V
I_D (at $V_{GS}=10V$)	44A	50A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	<11m Ω	<8.5m Ω
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	<14m Ω	<12m Ω

100% UIS Tested
 100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units	
Drain-Source Voltage	V_{DS}	30		V	
Gate-Source Voltage	V_{GS}	± 20	± 20	V	
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	44	50	A
		$T_C=100^\circ\text{C}$	28	32	
Pulsed Drain Current ^c	I_{DM}	100	140		
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	11	12	A
		$T_A=70^\circ\text{C}$	9	10	
Avalanche Current ^c	I_{AS}, I_{AR}	27	15	A	
Avalanche Energy $L=0.1\text{mH}$ ^c	E_{AS}, E_{AR}	36	11	mJ	
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	31	35	W
		$T_C=100^\circ\text{C}$	12.5	14	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	1.9	2.1	W
		$T_A=70^\circ\text{C}$	1.2	1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$	

Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	29	24	35	29	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	56	50	67	60
Maximum Junction-to-Case	$R_{\theta JC}$	3.4	3	4	3.6	$^\circ\text{C}/\text{W}$

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =125°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.5	2	2.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	100			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		8.8 12	11 15	mΩ
		V _{GS} =4.5V, I _D =20A		11.2	14	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		55		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.74	1	V
I _S	Maximum Body-Diode Continuous Current				35	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	920	1150	1380	pF
C _{oss}	Output Capacitance		125	180	235	pF
C _{rss}	Reverse Transfer Capacitance		60	105	150	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.55	1.1	1.65	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A	16	20	24	nC
Q _g (4.5V)	Total Gate Charge		7	9.5	11.4	nC
Q _{gs}	Gate Source Charge			2.7		nC
Q _{gd}	Gate Drain Charge			5		nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		6.5		ns
t _r	Turn-On Rise Time			2		ns
t _{D(off)}	Turn-Off Delay Time			17		ns
t _f	Turn-Off Fall Time			3.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs	7	8.7	10.5	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs	11	13.5	16	nC

A. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

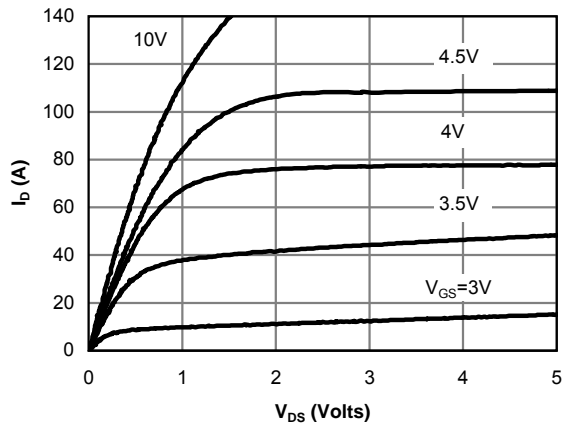


Figure 1: On-Region Characteristics (Note E)

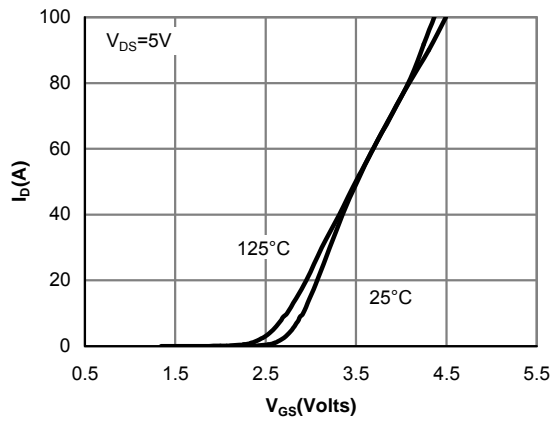


Figure 2: Transfer Characteristics (Note E)

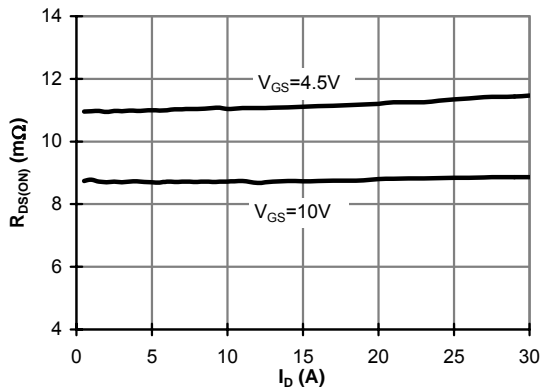


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

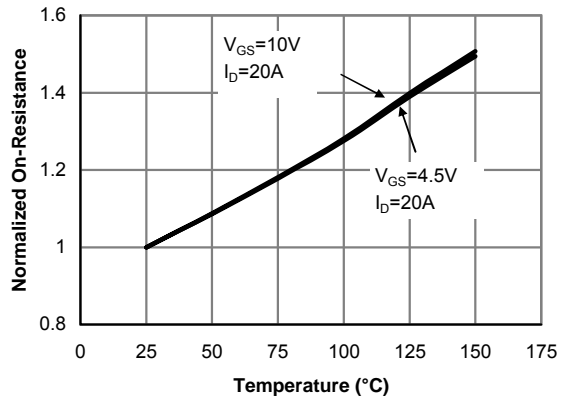


Figure 4: On-Resistance vs. Junction Temperature (Note E)

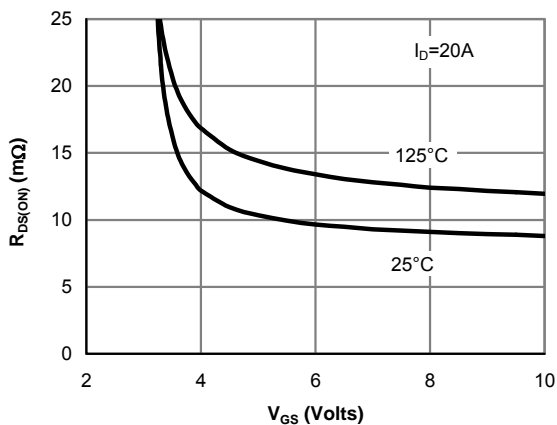


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

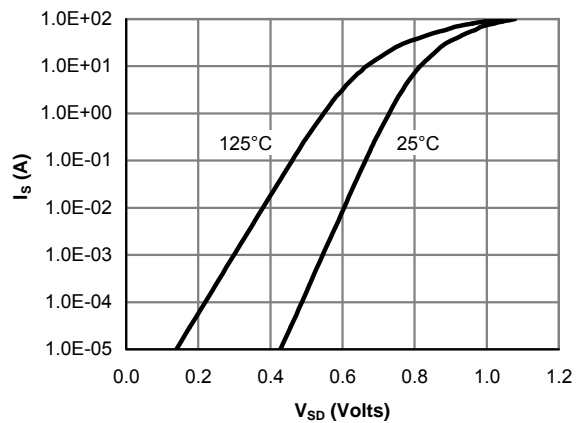


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

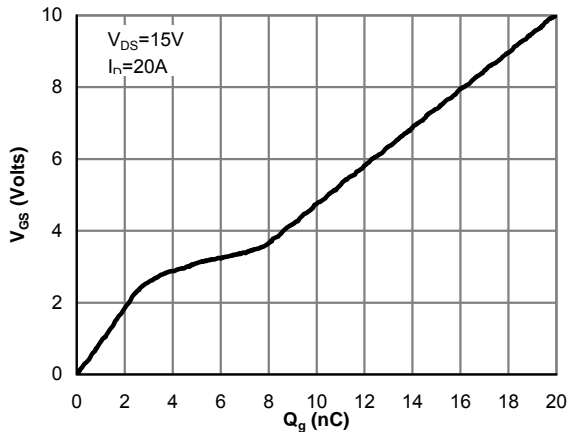


Figure 7: Gate-Charge Characteristics

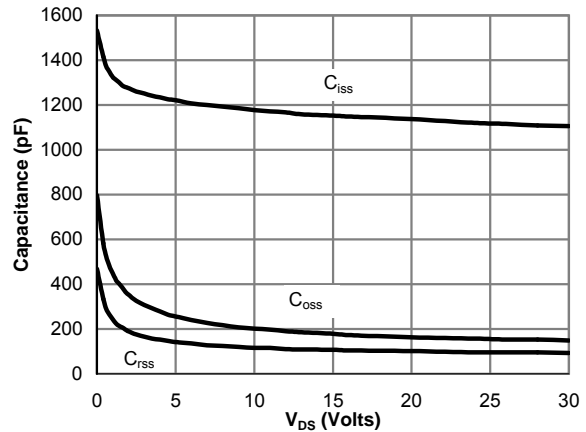


Figure 8: Capacitance Characteristics

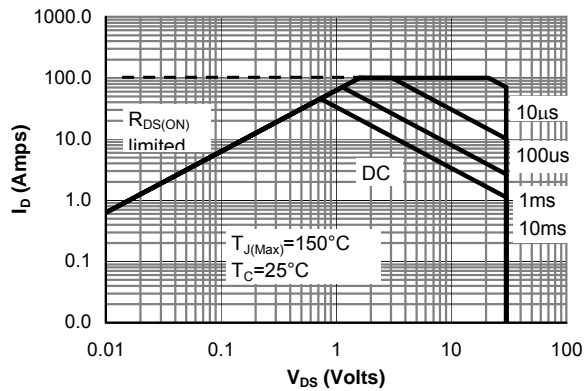


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

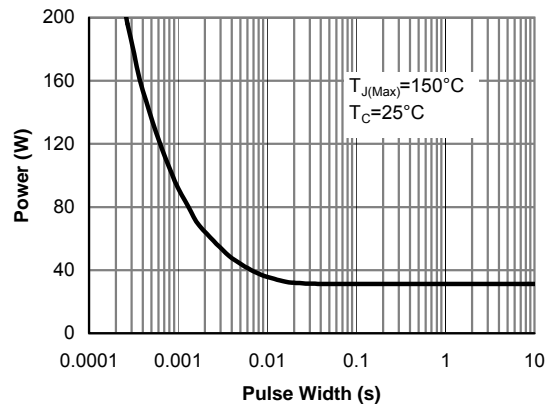


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

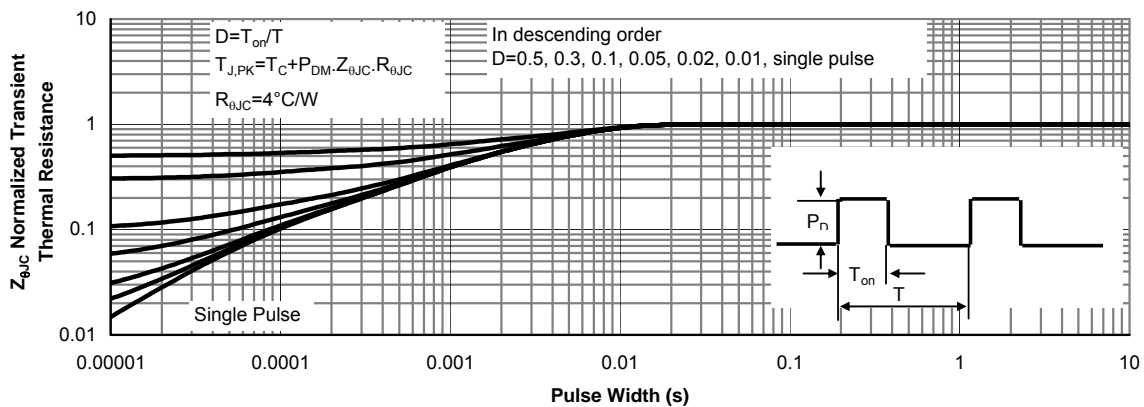


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

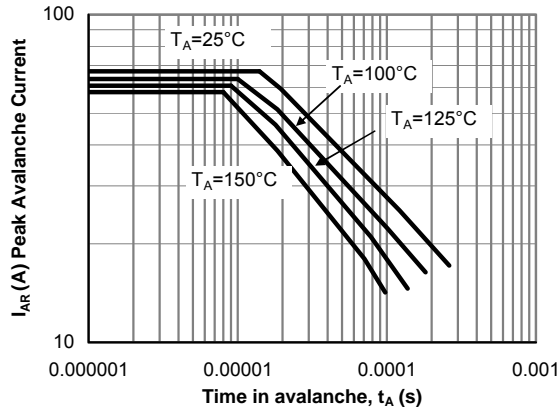


Figure 12: Single Pulse Avalanche capability (Note C)

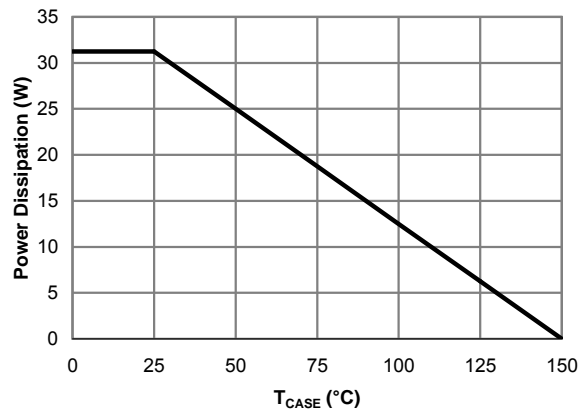


Figure 13: Power De-rating (Note F)

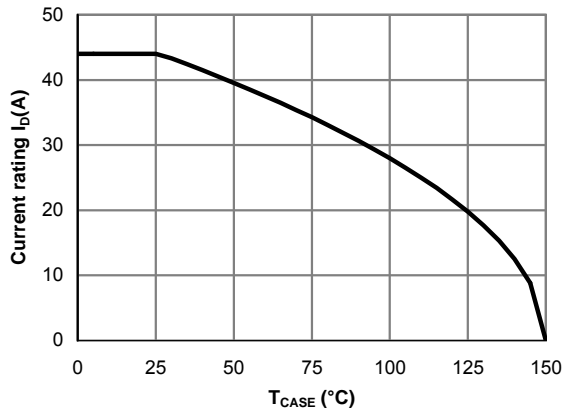


Figure 14: Current De-rating (Note F)

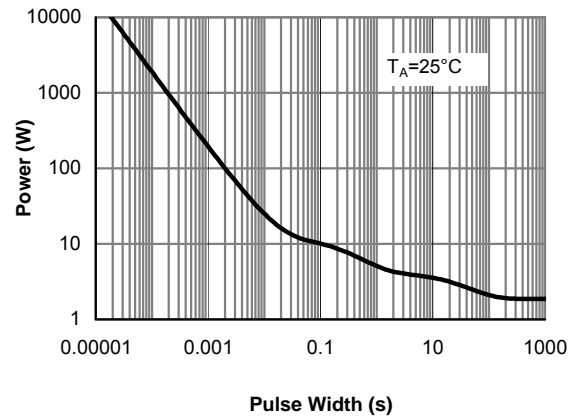


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

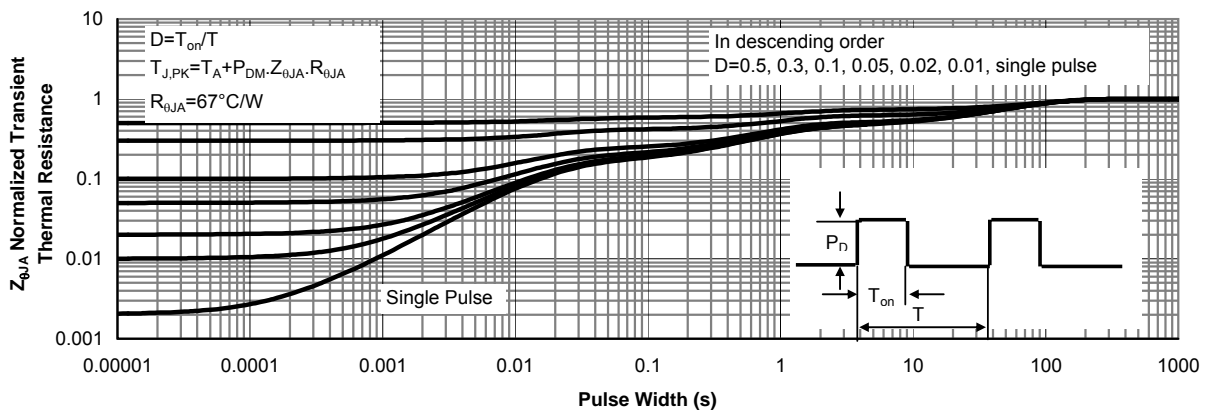


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =125°C			0.5 100	mA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.2	1.9	2.4	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	140			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		6.9 9.8	8.5 12	mΩ
		V _{GS} =4.5V, I _D =20A		9.3	12	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		50		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.5	0.7	V
I _S	Maximum Body-Diode Continuous Current				40	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	900	1130	1360	pF
C _{oss}	Output Capacitance		320	465	605	pF
C _{rss}	Reverse Transfer Capacitance		12	40	70	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.35	0.7	1.1	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A	12	16	20	nC
Q _g (4.5V)	Total Gate Charge		6	8	10	nC
Q _{gs}	Gate Source Charge			3		nC
Q _{gd}	Gate Drain Charge			3		nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			4		ns
t _{D(off)}	Turn-Off Delay Time			19		ns
t _f	Turn-Off Fall Time			3		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs	9	12	15	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs	18	23	28	nC

A. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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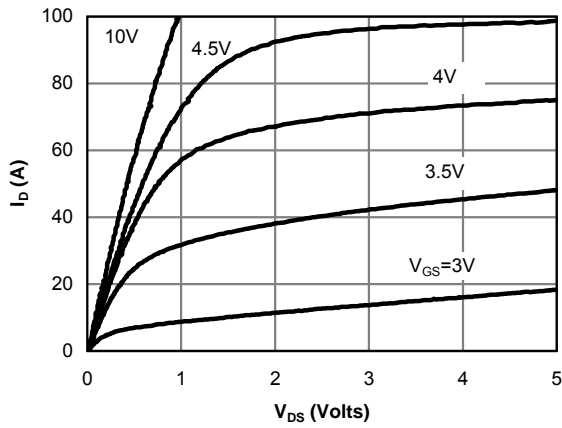


Fig 1: On-Region Characteristics (Note E)

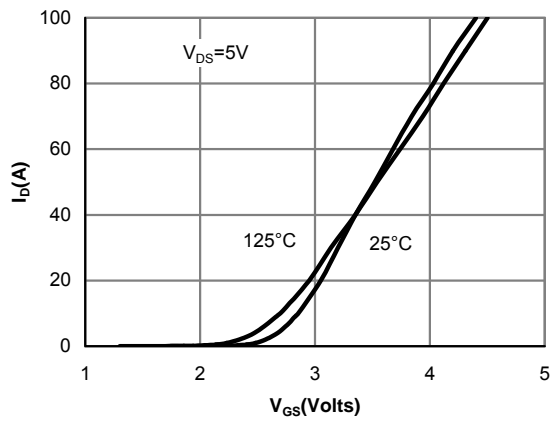


Figure 2: Transfer Characteristics (Note E)

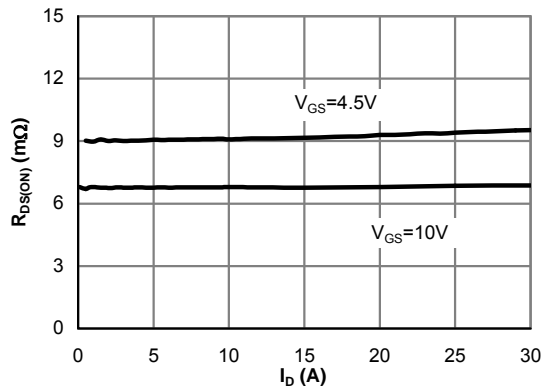


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

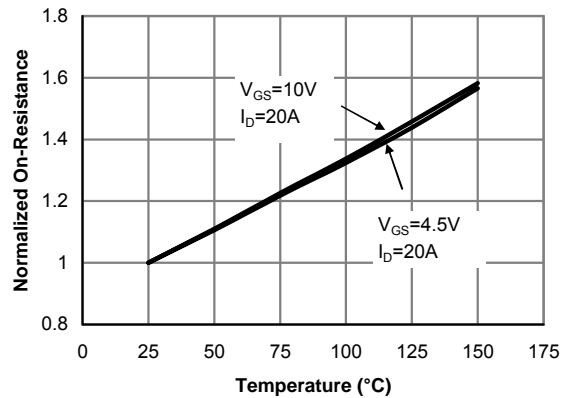


Figure 4: On-Resistance vs. Junction Temperature (Note E)

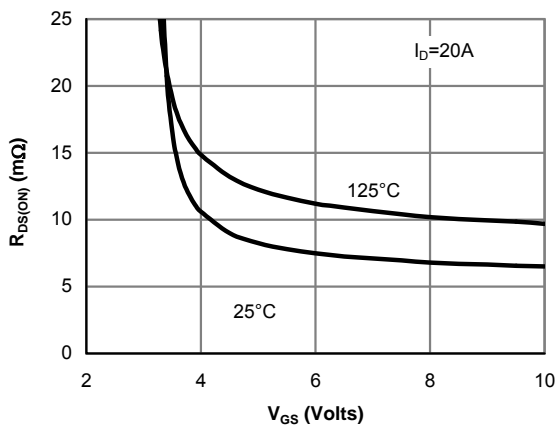


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

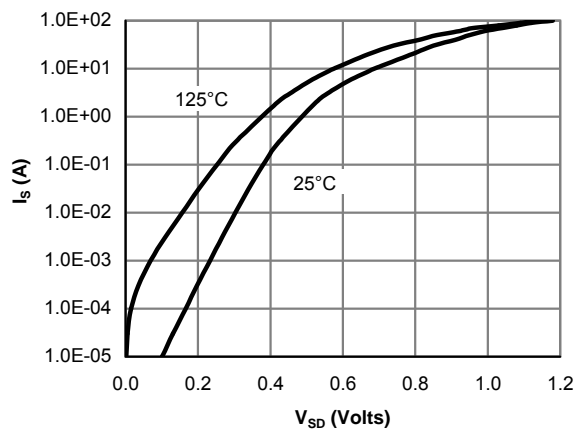


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

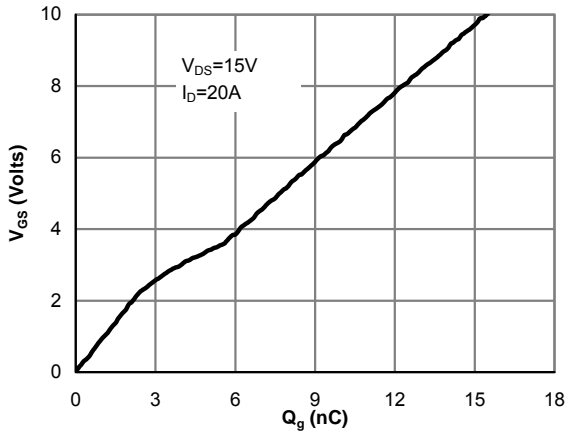


Figure 7: Gate-Charge Characteristics

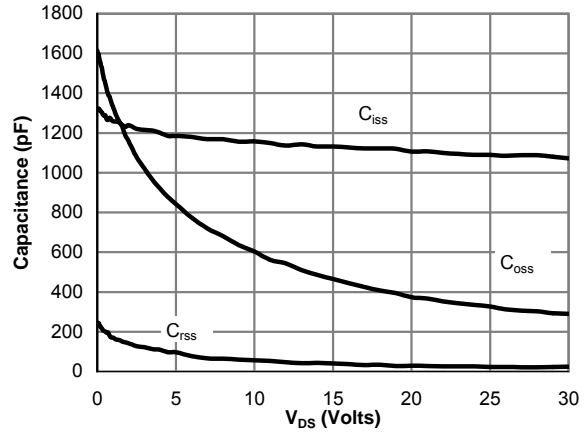


Figure 8: Capacitance Characteristics

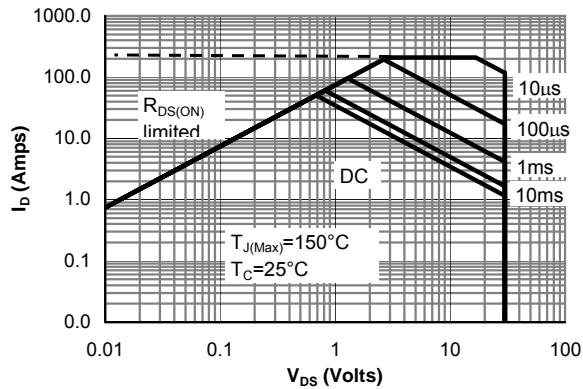


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

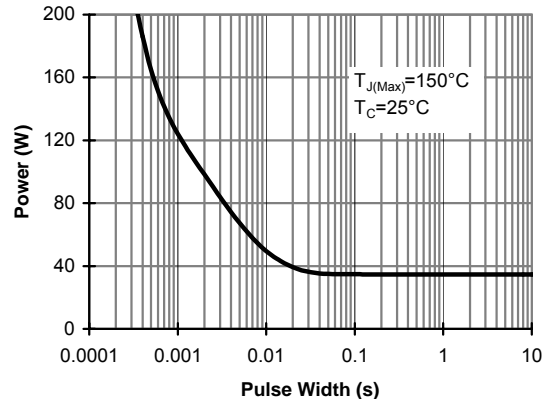


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

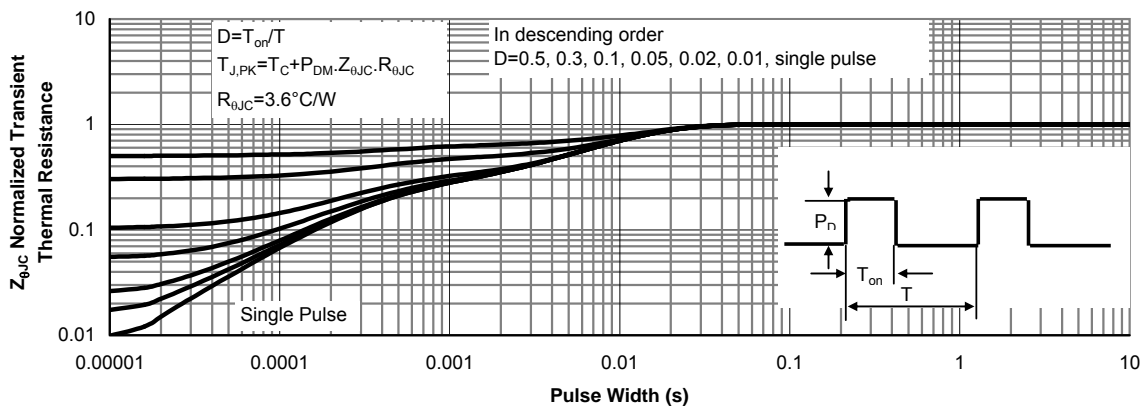


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

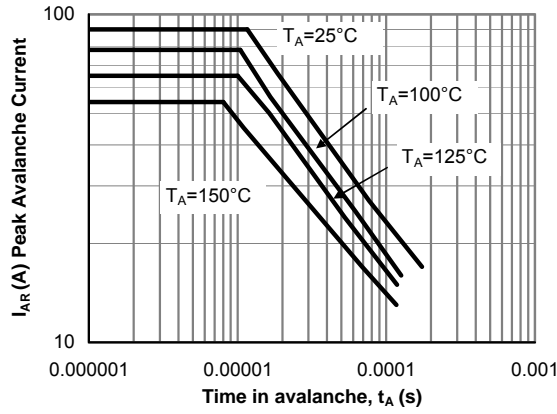


Figure 12: Single Pulse Avalanche capability (Note C)

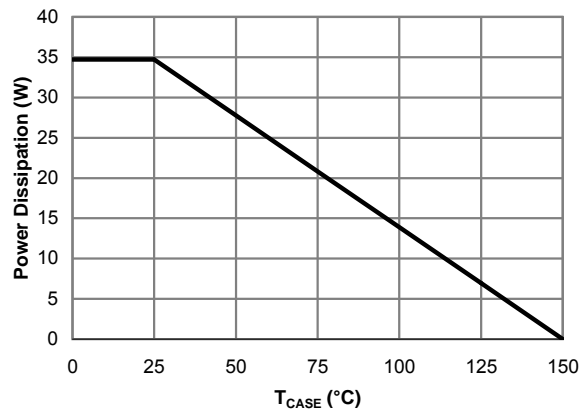


Figure 13: Power De-rating (Note F)

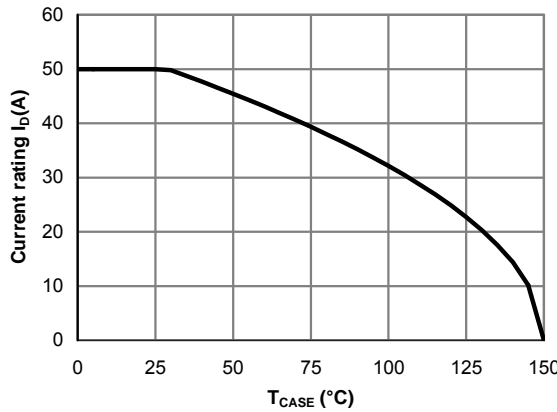


Figure 14: Current De-rating (Note F)

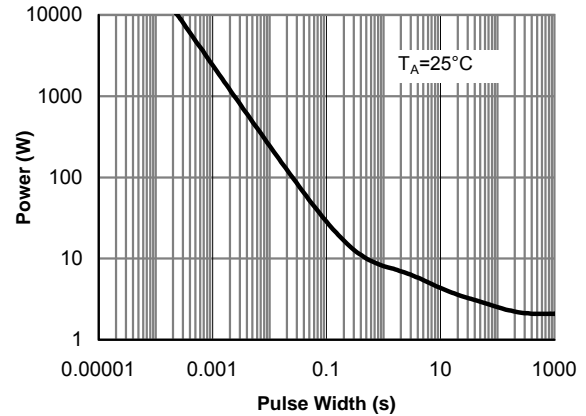


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

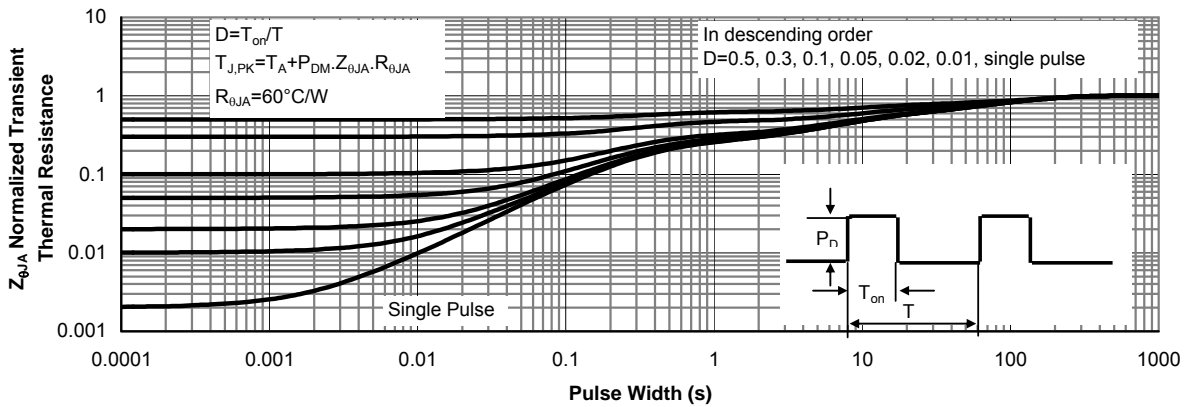
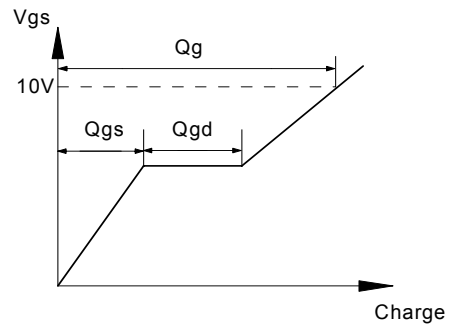
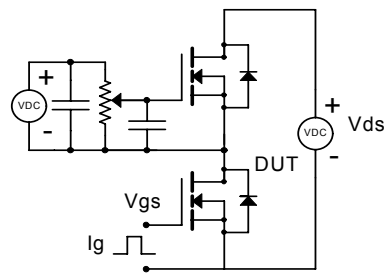
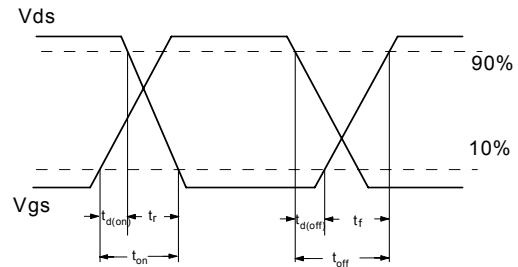
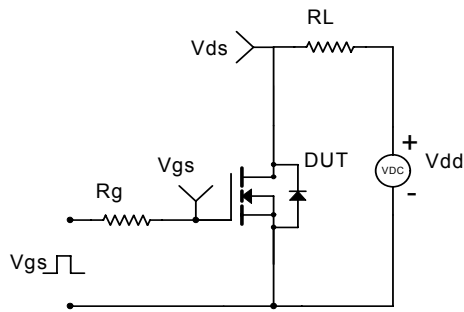


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

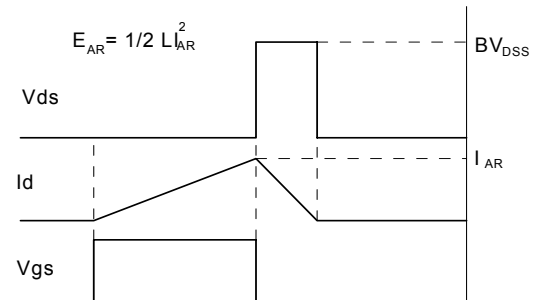
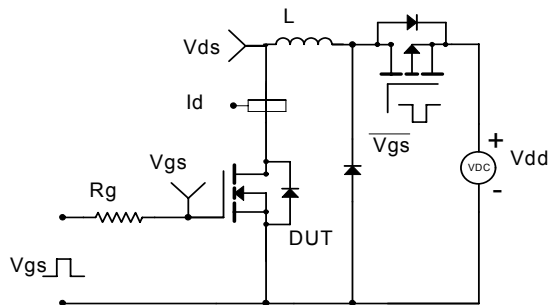
Gate Charge Test Circuit & Waveform



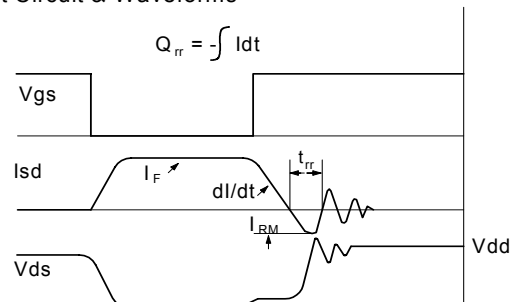
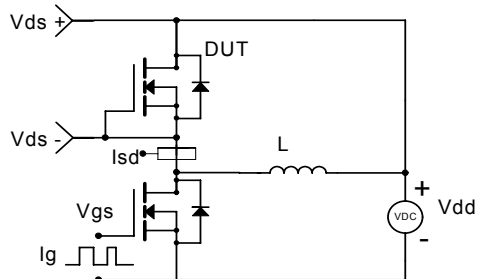
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